Claims

[c1] A memory device comprising:
a memory cell array having a plurality of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines and one of said second wordlines;
a first wordline decoder being coupled to said multitude of first wordlines to activate one of said wordlines;
a second wordline decoder being coupled to said multitude of wordlines to activate one of said second wordlines; and
a refresh control circuit arrangement including a contention circuit that allocates a refresh to one of said wordline decoders, whereby said one of said wordline decoders is currently not used for an external access to one of the memory cells of said memory cell array.

[c2] The memory device according to claim 1 wherein each of said first and second wordline decoders is designed to perform an access to one of said memory cells by enabling one of the multitude of said wordlines; wherein said contention circuit is designed to select said one of said first and second wordline decoders to perform a refresh operation to said memory cells connected to said multitude of wordlines coupled to said one of said first and second wordline decoders and is designed to select another one of said first and second wordline decoders to perform an external access.

[c3] The memory device according to claim 2 wherein said contention circuit is designed to issue a wait cycle for said one of said first and second decoders when said one wordline decoder receives an external request for an access.

[c4] The memory device according to claim 1 wherein said refresh control circuit arrangement comprises a refresh address counter that counts the addresses of the wordlines to be refreshed and comprises a comparator to compare said address of said wordline to be refresh with an address of a wordline to be accessed upon an external request, wherein in response to an address match a refresh cycle is suppressed.

[c5] The memory device according to claim 1 wherein a first access port and a second access port are provided; said first access port comprising said first wordline decoder and said second access port comprising said second wordline decoder; a terminal to provide a first select signal to enable an access through said first port and a terminal to provide a second port select signal to enable an access through said second port; said contention circuit providing an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if the port select signal provided to said first access port is activated and the port select signal provided to said second access port is deactivated.

[c6] The memory device according to claim 5 wherein said contention circuit provides an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if the port select signals provided to said first and second access ports are both activated, and wherein said contention circuit issues a wait signal to delay an externally requested access to a memory cell through said first access port during said refresh performed through said first access port.

[c7] The memory device according to claim 5 or 6 wherein said contention circuit is designed to perform a wait cycle for an externally requested access for one of said ports, if the first and the second port select signals are activated.

[c8] The memory device according to any of claims 1 to 7, wherein the memory cells each comprise a storage device having a first and a second terminal, a first access transistor connected to said first terminal and a second access transistor connected to said second terminal, said first access transistor connected to one of the multitude of said first wordlines and first bitlines, said second access transistor connected to one of the multitude of second wordlines and second bitlines.

[c9] A method of operating a memory device wherein said memory device has first and second access ports, memory cells being arranged in a multitude of rows, each row being accessible through said first and said second ports, and first and second row decoders decoding one of said rows in response to a respective

row address, wherein a refresh is performed on the memory cells of one of said rows by enabling said row through the first row decoder while another row is accessed in response to an externally requested access through the second row decoder.

[c10] The method according to claim 9 wherein a wait cycle for an externally requested access is issued for said one port of said first row decoder when the first and the second access ports each receive an externally requested access.

[c11] The method according to claim 9 further comprising the step of counting the row address of rows to be refreshed and suppressing a refresh of the memory cells of a row when a row address of an externally requested access and the row address of said row to be refreshed match each other.